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CAMPOS, YAIMA	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/683,688	YAMAMOTO ET AL.	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/17/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/683,688 has a total of 20 claims pending in the application; there are 4 independent claims and 16 dependent claims, all of which are ready for examination by the examiner.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 27, 2006 has been entered.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

4. As required bye **M.P.E.P. 201.14(c)**, acknowledgement is made of applicant's claim for priority based on an application filed on June 23, 2003 (Foreign Priority 2003-177451).

III. INFORMATION CONCERNING DRAWINGS

Drawings

5. The applicant's drawings submitted are acceptable for examination purposes.

IV. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

6. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated May 27, 2006 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

V. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. **Claim 1-8, 11 and 19** are rejected under 35 U.S.C. 102(e) as being anticipated by Fukuzawa et al. (US 6,529,976).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

1. As per **claims 1, 11 and 19**

"A storage system that is connected to a computer and another storage system including a first storage device, the storage system provides a logical volume which corresponds to a storage device in the storage system or the another storage system transparent from the computer, the storage system comprising:" as **["Processing system A 100" connected to "processing system B 110" and "processing system X 120" (Figure 2) and explains "a mainframe is capable of accessing a memory of an I/O subsystem of an open system not directly connected to the mainframe... wherein the first I/O subsystem includes a table for storing a device address of an external memory, data indicating one of the external memory of the first I/O subsystem and the external memory of the second I/O subsystem to which the device address is assigned... wherein upon receipt of a read/write request...from the first host computer and including an address of an external memory to be read from or written into, and upon decision, with reference to the table, that the request is assigned to the external memory included in the second I/O subsystem converts the read/write request into a second**

read/write request...and sends the second read/write request to the second I/O subsystem" (Column 2, line 8 – Column 4, line 57). Fukuzawa also explains using virtual/logical data addressing (Column 6, lines 47-61)]

"a first control section that is connected to the computer;" **[Fukuzawa discloses this limitation as "Disk controller X 123" in "processing system X 120" connected to "open system host X" (Figure 2)]**

"a second control section that includes a second storage device that stores data to be used by the computer and a cache memory, that temporarily stores data form the first control section before storing the data in the second storage device;" **[With respect to this limitation, Fukuzawa discloses "Processing system A 100" having "Disk controller A 104" (Figure 2) and "mainframe 101" and shows the internal structure of each controller having "disk/cache device 304" (Figure 3)]**

"a third control section that is connected to the another storage system which includes another cache memory for temporarily storing data before storing the data in the first storage device;" **[With respect to this limitation, Fukuzawa discloses "Processing system B 110" having "Disk controller B 113" (Figure 2) and shows the internal structure of each controller having "disk/cache device 304" (Figure 3)]**

"and an internal network that mutually connects the first control section, the second control section and the third control section," **[With respect to this limitation, Fukuzawa discloses "communication line 108" (Figures 1 and 2; Column 6, lines 17-19)]**

"wherein the first control section receives from the computer a first input/output request having first identification information indicative of the logical volume to be accessed, and selects one of

the second control section or the third control section based on the first identification information, and sends a second input/output request corresponding to the first input/output request to the second control section or the third control section" **[Fukuzawa discloses this concept in an embodiment wherein "mainframe 101 and the hosts 111 and 121 for the open system access the magnetic tape library 107 constituting an external memory or the disk drive group A 105, the disk drive group B 114 and the disk drive group X 124 through each interface. The process of the mainframe 101 establishes a route to the data stored externally through each interface" (Figure 1; Column 6, lines 47-61) and explains "the device address 400 is an identifier (ID) for discriminating a disk device to be read from or written into by a host computer" (Column 7, lines 26-30) Also see (Column 8, line 41 – Column 10, line 34)]**.

2. As per **claim 2**, Fukuzawa discloses the storage system according to claim 1, **[See rejection to claim 1 above]** "wherein the first identification information is correlated to the second storage device, and the first control section converts the first input/output request to the second input/output request having identification information of the second control section, and transmits the second input/output request to the second control section" **[Fukuzawa discloses this concept as "a mainframe is capable of accessing a memory of an I/O subsystem of an open system not directly connected to the mainframe... wherein the first I/O subsystem includes a table for storing a device address of an external memory, data indicating one of the external memory of the first I/O subsystem and the external memory of the second I/O subsystem to which the device address is assigned... wherein upon receipt of a read/write request...from the first host computer and including an address of an external memory to**

be read from or written into, and upon decision, with reference to the table, that the request is assigned to the external memory included in the second I/O subsystem converts the read/write request into a second read/write request...and sends the second read/write request to the second I/O subsystem" (Column 2, line 8 – Column 4, line 57; Column 9, lines 21-23)].

3. As per **claim 3**, Fukuzawa discloses "A storage system according to claim 1," **[See rejection to claim 1 above]** "wherein the first identification information is correlated to the first storage device, and the first control section selects one of the second control section and the third control section to which the second input/output request is transmitted" **[Fukuzawa discloses this concept as "the device address 400 is an identifier (ID) for discriminating a disk device to be read from or written into by a host computer" (Column 7, lines 26-30) Also see (Column 8, line 41 – Column 10, line 34)" and explains that "in the case where the disk drive is connected to the disk controller A104...step 702 reads the corresponding data form the particular disk drive" but when the disk drive is an external drive, "then the address of the disk controller (disk controller B 113) actually connected to the designated disk drive and the address of the disk drive in the disk drive group B connected to the particular disk controller B113 are acquired on the basis of the remote controller-connected disk data 315" (Column 8, line 41 – Column 10, line 34)]**.

4. As per **claim 4**, Fukuzawa discloses a storage system according to claim 3, **[See rejection to claim 3 above]** "wherein the first control section transmits the second input/output request having the identification information of the second control section to the second control section when a processing concerning the first input/output request is executed by the second

control section" **[With respect to this limitation, Fukuzawa "upon receipt of a read/write request...from the first host computer and including an address of an external memory to be read from or written into, and upon decision, with reference to the table, that the request is assigned to the external memory included in the second I/O subsystem converts the read/write request into a second read/write request...and sends the second read/write request to the second I/O subsystem" (Column 2, line 8 – Column 4, line 57) (Column 8, line 41 – Column 10, line 34)]**.

5. As per **claims 5-8**, Fukuzawa discloses a storage system according to claims 3 and 4, **[See rejection to claims 3 and 4 above]** "wherein the second control section receives the second input/output request, converts the second input/output request to a third input/output request having identification information of the first storage system, and transmits the third input/output request to the third control section"

"the first control section transmits the second input/output request having identification information of the third control section to the third control section, when a processing concerning the first input/output request is not executed by the second control section" **[Fukuzawa discloses this concepts as "a mainframe is capable of accessing a memory of an I/O subsystem of an open system not directly connected to the mainframe... wherein the first I/O subsystem includes a table for storing a device address of an external memory, data indicating one of the external memory of the first I/O subsystem and the external memory of the second I/O subsystem to which the device address is assigned... wherein upon receipt of a read/write request...from the first host computer and including an address of an external memory to be read from or written into, and upon decision, with reference to the table, that the**

request is assigned to the external memory included in the second I/O subsystem converts the read/write request into a second read/write request...and sends the second read/write request to the second I/O subsystem" (Column 2, line 8 – Column 4, line 57) also see (Column 8, line 41 – Column 10, line 34) and explains that "three or more instead of two I/O subsystems can be connected" (Column 10 , lines 24-32)].

6. **Claims 1-20** are rejected under 35 U.S.C. 102(b) as being anticipated by Fujimoto, Kazuhisa (EP 1 132 805).

7. As per **claims 1, 11 and 19**, Fujimoto discloses

"A storage system that is connected to a computer and another storage system including a first storage device, the storage system provides a logical volume which corresponds to a storage device in the storage system or the another storage system transparent from the computer, the storage system comprising:" as **[With respect to this limitation, Fujimoto discloses "1-1:Disk array control unit" connected to "50: Host computer" and explains that "a disk array controller 1... is made up of multiple disk array control units 1-1..." wherein "one disk array control unit... can operate as a stand-alone disk array controller" (Figure 1; Column 7, Paragraph 0036-Column 8, Paragraph 0038; Column 7, Paragraph 0033) and explains that "the microprocessors 101 in the channel IF unit 11 which has received the request makes access to both shared memory units 13 in both disk array control units 1-1-1 and 1-1-2 thereby to find as to which hard disk drive 5 stores the requested data. The search is executed based on the conversion table stored in the shared memory units 13...the microprocessors 101 in the channel IF unit11 which has received the request makes access to both shared memory units 13 in both disk array control units 1-1-1 and 1-1-2 thereby to**

find as to whether or not the requested data is present in the cache memory units 14 in the disk array control units 1-1-1 and 1-1-2...In one case of finding the requested data in the cache memory unit 14 of the disk array control unit 1-1-1, the data is transferred...in other case of finding the data in the cache memory unit 14 of the disk array control unit 1-1-2, the data is transferred...In the case the request data does not exists in any cache memory unit 14, the microprocessor 101 issues a command to another microprocessors 101" wherein "the host computer 50 can deal with the multiple disk array control units 1-1 virtually as a single disk array controller 1" (Figure 8; Column 11, Paragraph 0057 – Column 12, Paragraph 0065; Embodiment 1) and discloses another embodiment in which "the shared memory unit 13 in other disk array control unit 1-2 takes place via the shared memory unit 13 in the self unit 1-2 and the interconnection 24" (Column 14, Paragraph 0077-0078; Embodiment2). Further disclosing a third embodiment in which "access to the cache memory unit 14 in other disk array control unit 1-3 takes place via the cache memory unit 14 in the self unit 1-3 and the interconnection 25... in the case of reading out data from a hard disk drive 5 connected to a disk array control unit 1-3 which is different from the unit 1-3 that has received the request, the data can be read out by way of internal interconnection and cache memory unit 14, instead of moving the data through the channel IF units 11 of both disk array control units 1-3" (Column 16, Paragraphs 0094-0096; Embodiment 3)]

"a first control section that is connected to the computer;" **["control unit 1-1" (Figure 8)]**

"a second control section that includes a second storage device that stores data to be used by the computer and a cache memory, that temporarily stores data form the first control section before

storing the data in the second storage device;" **[With respect to this limitation, Fujimoto discloses "control unit 1-1-2" having "cache memory unit 14" which stores data pertaining to "hard disk drive 5" connected to "disk array control unit 1-1-2" (Figure 8; Figure 11; Column 11, Paragraph 0057 –Column 12, Paragraph 0065)]**

"a third control section that is connected to the another storage system which includes another cache memory for temporarily storing data before storing the data in the first storage device;" **[With respect to this limitation Fujimoto discloses "the array controller shown in Fig. 8 will be able to include three or more disk array control units" (Column 10, Paragraphs 0053-0054; Figure 19)]**

"and an internal network that mutually connects the first control section, the second control section and the third control section," **[Fujimoto discloses this limitation as "as a preferred embodiment of this invention, the channel interface units and disk interface units and the cache memory units in the multiple disk array control units are interconnected by a switch-based interconnection" (Figures 1, 7 and 8; Column 6, Paragraph 0030)]**

"wherein the first control section receives from the computer a first input/output request having first identification information indicative of the logical volume to be accessed, and selects one of the second control section or the third control section based on the first identification information, and sends a second input/output request corresponding to the first input/output request to the second control section or the third control section" **[With respect to this limitation, Fujimoto discloses and embodiment in which "access to the cache memory unit 14 in other disk array control unit 1-3 takes place via the cache memory unit 14 in the self unit 1-3 and the interconnection 25... in the case of reading out data from a hard disk drive**

5 connected to a disk array control unit 1-3 which is different from the unit 1-3 that has received the request, the data can be read out by way of internal interconnection and cache memory unit 14, instead of moving the data through the channel IF units 11 of both disk array control units 1-3" (Column 16, Paragraphs 0094-0096; Embodiment 3) (Embodiment 3, Column 14, Paragraph 0080-Column 18, Paragraph 0013)].

8. As per **claim 2**, Fujimoto discloses a storage system according to claim 1, **[See rejection to claim 1 above]** 'wherein the first identification information is correlated to the second storage device, and the first control section converts the first input/output request to the second input/output request having identification information of the second control section, and transmits the second input/output request to the second control section" **[Fujimoto discloses this concept as "an original data set is stored on the hard disk drive 5 connected to the disk array control unit 1-1-1 and a duplicate data set is stored on the hard disk drive 5 connected to the disk array control unit 1-1-2 in Fig. 8" (Column 17, Paragraph 0099-0100) "the command receiving microprocessor 101 reads out the updated data from the hard disk drive 5 and converts the addresses of updated data into addresses of duplicate data" (Column 18, Paragraph 0102)]**.

9. As per **claims 3 and 4**, Fujimoto discloses a storage system according to claim 1, **[See rejection to claim 1 above]"** wherein the first identification information is correlated to the first storage device, and the first control section selects one of the second control section and the third control section to which the second input/output request is transmitted" and "the first control section transmits the second input/output request having the identification information of the second control section to the second control section when a processing concerning the first

input/output request is executed by the second control section. **[With respect to this limitation, Fujimoto discloses "function of moving data which is accessed frequently by one host computer 50 and is stored on a hard disk drive connected to a disk array control unit other that n the control unit connected to the one host computer 50, to the hard disk drive of the control unit connected to the one host computer" (Columns 19-20, Paragraphs 0110-0117) and also explains that "the microprocessors 101 in the channel IF unit 11 which has received the request makes access to both shared memory units 13 in both disk array control units 1-1-1 and 1-1-2 thereby to find as to which hard disk drive 5 stores the requested data. The search is executed based on the conversion table stored in the shared memory units 13...the microprocessors 101 in the channel IF unit11 which has received the request makes access to both shared memory units 13 in both disk array control units 1-1-1 and 1-1-2 thereby to find as to whether or not the requested data is present in the cache memory units 14 in the disk array control units 1-1-1 and 1-1-2...In one case of finding the requested data in the cache memory unit 14 of the disk array control unit 1-1-1, the data is transferred...in other case of finding the data in the cache memory unit 14 of the disk array control unit 1-1-2, the data is transferred...In the case the request data does not exists in any cache memory unit 14, the microprocessor 101 issues a command to another microprocessors 101" wherein "the host computer 50 can deal with the multiple disk array control units 1-1 virtually as a single disk array controller 1" (Figure 8; Column 11, Paragraph 0057 – Column 12, Paragraph 0065; Embodiment 1) and discloses another embodiment in which "the shared memory unit 13 in other disk array control unit 1-2 takes place via the shared memory unit 13 in the self unit 1-2 and the interconnection 24"**

(Column 14, Paragraph 0077-0078; Embodiment2). Further disclosing a third embodiment in which "access to the cache memory unit 14 in other disk array control unit 1-3 takes place via the cache memory unit 14 in the self unit 1-3 and the interconnection 25... in the case of reading out data from a hard disk drive 5 connected to a disk array control unit 1-3 which is different from the unit 1-3 that has received the request, the data can be read out by way of internal interconnection and cache memory unit 14, instead of moving the data through the channel IF units 11 of both disk array control units 1-3" (Column 16, Paragraphs 0094-0096; Embodiment 3)].

10. As per **claims 5-8**, Fujimoto discloses a storage system according to claims 3 and 4, **[See rejection to claims 3 and 4 above]** "wherein the second control section receives the second input/output request, converts the second input/output request to a third input/output request having identification information of the first storage system, and transmits the third input/output request to the third control section" and "the first control section transmits the second input/output request having identification information of the third control section to the third control section, when a processing concerning the first input/output request is not executed by the second control section" **[With respect to this limitation, Fujimoto discloses "the microprocessors 101 issues a command by way of the shared memory unit 13 of the disk array control unit 1-1-1 to the microprocessor 101 in the disk IF unit 12 which is connected to the hard disk drive 5 where the original data set is stored, thereby operating on it to read out data from the cache memory unit 14 of the disk array control unit 1-1-1, transfers the data to the disk IF unit 12 which is connected to the hard disk drive 5 where the original**

data set is stored, and operates the disk IF unit 12 to transfer and write the data onto the hard disk drive 5" (Column 17, Paragraph 0100)].

11. As per **claims 9, 12-15 and 17-18 and 20**, Fujimoto discloses a storage system according to claims 3, 11, 16 and 19, **[See rejection to claims 3, 11 and 19 above and rejection to claim 16 bellow]** "further comprising: a management adaptor that manages the first control section, the second control section and the third control section, wherein the management adaptor manages identification information of a storage device correlated to the first identification information" **[With respect to this limitation, Fujimoto discloses "SM-SWs 110 and CM-SWs 111" which "have the function of directing access requests from the channel IF units 11 and disk IF units 12 over the four access paths to the two access paths of the shared memory units 13 or cache memory units 14 within the self disk array control unit 1-1 and the two inter-unit access paths of the shared memory units 13 or cache memory units 14 of other disk array control unit 1-1" (Column 10, Paragraph 0049; Column 7, Paragraph 0036-Column 12, Paragraph 0065)]**. Fujimoto further explains **["function of moving data which is accessed frequently by one host computer 50 and is stored on a hard disk drive connected to a disk array control unit other that n the control unit connected to the one host computer 50, to the hard disk drive of the control unit connected to the one host computer" (Columns 19-20, Paragraphs 0110-0117) and also explains that "the microprocessors 101 in the channel IF unit 11 which has received the request makes access to both shared memory units 13 in both disk array control units 1-1-1 and 1-1-2 thereby to find as to which hard disk drive 5 stores the requested data. The search is executed based on the conversion table stored in the shared memory units 13...the microprocessors 101 in the channel IF unit11 which has**

received the request makes access to both shared memory units 13 in both disk array control units 1-1-1 and 1-1-2 thereby to find as to whether or not the requested data is present in the cache memory units 14 in the disk array control units 1-1-1 and 1-1-2...In one case of finding the requested data in the cache memory unit 14 of the disk array control unit 1-1-1, the data is transferred...in other case of finding the data in the cache memory unit 14 of the disk array control unit 1-1-2, the data is transferred...In the case the request data does not exists in any cache memory unit 14, the microprocessor 101 issues a command to another microprocessors 101" wherein "the host computer 50 can deal with the multiple disk array control units 1-1 virtually as a single disk array controller 1" (Figure 8; Column 11, Paragraph 0057 – Column 12, Paragraph 0065; Embodiment 1) and discloses another embodiment in which "the shared memory unit 13 in other disk array control unit 1-2 takes place via the shared memory unit 13 in the self unit 1-2 and the interconnection 24" (Column 14, Paragraph 0077-0078; Embodiment2). Further disclosing a third embodiment in which "access to the cache memory unit 14 in other disk array control unit 1-3 takes place via the cache memory unit 14 in the self unit 1-3 and the interconnection 25... in the case of reading out data from a hard disk drive 5 connected to a disk array control unit 1-3 which is different from the unit 1-3 that has received the request, the data can be read out by way of internal interconnection and cache memory unit 14, instead of moving the data through the channel IF units 11 of both disk array control units 1-3" (Column 16, Paragraphs 0094-0096; Embodiment 3)].

1. As per **claim 10**, Fujimoto discloses a storage system according to claim 9, **[See rejection to claim 9 above]** "wherein the management adaptor manages identification

information of the first storage device and identification information of the second control section being correlated to the first identification information, and the first control section converts the first input/output request to the second input/output request having identification information of the second control section, and transmits the second input/output to the second control section" **[Fujimoto discloses this concept as "an original data set is stored on the hard disk drive 5 connected to the disk array control unit 1-1-1 and a duplicate data set is stored on the hard disk drive 5 connected to the disk array control unit 1-1-2 in Fig. 8" (Column 17, Paragraph 0099-0100) "the command receiving microprocessor 101 reads out the updated data from the hard disk drive 5 and converts the addresses of updated data into addresses of duplicate data" (Column 18, Paragraph 0102)]**.

2. As per **claim 16**, Fujimoto discloses

"A second storage system that is connected to a computer and a first storage system including a first storage device, the second storage system comprising:" **[With respect to this limitation, Fujimoto discloses "1-1:Disk array control unit" connected to "50: Host computer" and explains that "a disk array controller 1... is made up of multiple disk array control units 1-1..." wherein "one disk array control unit... can operate as a stand-alone disk array controller" (Figure 1; Column 7, Paragraph 0036-Column 8, Paragraph 0038; Column 7, Paragraph 0033)]**

"a first control section that is connected to the computer;" **[Fukuzawa discloses this limitation as "Disk controller X 123" in "processing system X 120" connected to "open system host X" (Figure 2)]**

"a second control section that includes a second storage device and a cache memory;" **[With respect to this limitation, Fukuzawa discloses "Processing system A 100" having "Disk controller A 104" (Figure 2) and "mainframe 101" and shows the internal structure of each controller having "disk/cache device 304" (Figure 3)]**

"a third control section that is connected to the first storage system;" **[With respect to this limitation Fujimoto discloses "the array controller shown in Fig. 8 will be able to include three or more disk array control units" (Column 10, Paragraphs 0053-0054; Figure 19)]**

"an internal network that mutually connects the first control section, the second control section and the third control section," **[Fujimoto discloses this limitation as "as a preferred embodiment of this invention, the channel interface units and disk interface units and the cache memory units in the multiple disk array control units are interconnected by a switch-based interconnection" (Figures 1, 7 and 8; Column 6, Paragraph 0030)]**

"wherein the first control section receives from the computer an input/output request to the first storage device, and the first control section selects if the input/output request is transmitted to the first storage system via a first path defined by the internal network and the third control section or if the Input/output request is transmitted to the first storage system via a second path defined by the internal network and the second control section and the third control section;" **["the microprocessors 101 in the channel IF unit 11 which has received the request makes access to both shared memory units 13 in both disk array control units 1-1-1 and 1-1-2 thereby to find as to which hard disk drive 5 stores the requested data. The search is executed based on the conversion table stored in the shared memory units 13...the microprocessors 101 in the channel IF unit11 which has received the request makes access to both shared memory**

units 13 in both disk array control units 1-1-1 and 1-1-2 thereby to find as to whether or not the requested data is present in the cache memory units 14 in the disk array control units 1-1-1 and 1-1-2...In one case of finding the requested data in the cache memory unit 14 of the disk array control unit 1-1-1, the data is transferred...in other case of finding the data in the cache memory unit 14 of the disk array control unit 1-1-2, the data is transferred...In the case the request data does not exists in any cache memory unit 14, the microprocessor 101 issues a command to another microprocessors 101" wherein "the host computer 50 can deal with the multiple disk array control units 1-1 virtually as a single disk array controller 1" (Figure 8; Column 11, Paragraph 0057 – Column 12, Paragraph 0065; Embodiment 1) and discloses another embodiment in which "the shared memory unit 13 in other disk array control unit 1-2 takes place via the shared memory unit 13 in the self unit 1-2 and the interconnection 24" (Column 14, Paragraph 0077-0078; Embodiment2). Further disclosing a third embodiment in which "access to the cache memory unit 14 in other disk array control unit 1-3 takes place via the cache memory unit 14 in the self unit 1-3 and the interconnection 25... in the case of reading out data from a hard disk drive 5 connected to a disk array control unit 1-3 which is different from the unit 1-3 that has received the request, the data can be read out by way of internal interconnection and cache memory unit 14, instead of moving the data through the channel IF units 11 of both disk array control units 1-3" (Column 16, Paragraphs 0094-0096; Embodiment 3)]

"and a management adaptor that manages the first control section, the second control section and the third control section, and is connected to the internal network, wherein, when the third

control section is connected to the first storage system, the management adaptor sets to transmit to the first storage system an input/output request to the first storage device via one of the first path or the second path wherein, when the management adaptor sets to change a path that is used to transmit an input/output request to the first storage device from the second path to the first path," **[With respect to this limitation, Fujimoto discloses "SM-SWs 110 and CM-SWs 111" which "have the function of directing access requests from the channel IF units 11 and disk IF units 12 over the four access paths to the two access paths of the shared memory units 13 or cache memory units 14 within the self disk array control unit 1-1 and the two inter-unit access paths of the shared memory units 13 or cache memory units 14 of other disk array control unit 1-1" (Column 10, Paragraph 0049; Column 7, Paragraph 0036-Column 12, Paragraph 0065)]**. Fujimoto further explains **["function of moving data which is accessed frequently by one host computer 50 and is stored on a hard disk drive connected to a disk array control unit other that n the control unit connected to the one host computer 50, to the hard disk drive of the control unit connected to the one host computer" (Columns 19-20, Paragraphs 0110-0117)]**

"wherein the second control section controls to store data, that is stored in the cache memory and is to be stored in the first storage device to the first storage device, so that a storage region on the cache memory is released, and wherein after the storage region on the cache memory is released, the management adaptor changes the path that is used to transmit an input/output request to the first storage system" **[With respect to this limitation, Fujimoto discloses "in the case the request data does not exist in any cache memory unit 14, the microprocessor 101 issues a command to another microprocessor 101 in the disk IF units 12 which is connected with**

the hard disk drive 5 where the requested data is stored" (Column 11, Paragraph 0061). Applicant should note that data might not be in cache due to a cache flush operation. Furthermore, Fujimoto explains that "the disk IF unit implements the data transfer between cache memories. The function of data transfer between cache memory units 14 of different disk array control units 1-3 is necessary for moving data to a disk array control unit of less-frequent access in dealing with concentrated access from host computers 50 to one disk array control unit 1-3" (Column 15, Paragraph 0083); therefore, only the most frequently accessed data is maintained in cache and when the cache is flushed, data will no longer be in cache, and "In the case the request data does not exists in any cache memory unit 14, the microprocessor 101 issues a command to another microprocessors 101" wherein "the host computer 50 can deal with the multiple disk array control units 1-1 virtually as a single disk array controller 1" (Figure 8; Column 11, Paragraph 0057 – Column 12, Paragraph 0065; Embodiment 1) (See embodiments 1-3 in Column 7, Paragraph 36 – Column 16, Paragraph 0096) and explains "in the event of a fault on one access path or in one SM-SW 110, the shared memory units13 are kept accessible through another route" (Column 9, Paragraph 0045). Fujimoto also explains that "in case the request data does not exist in any cache memory unit 14, the microprocessor 101 issues a command to another microprocessor 101 in the disk IF units 12 which is connected with the hard disk drive 5 where the requested data is stored, thereby operating it to read out and store the data from the hard disk drive 5 into one cache memory unit 14" (Column 11, Paragraph 0061)].

VI. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

10. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

11. Per the instant office action, claims 1-20 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

13. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Donald Sparks, can be reached at the following telephone number: Area Code (571) 272-4201.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

August 2, 2006

Yaima Campos
Examiner
Art Unit 2185

DONALD SPARKS
SUPERVISORY PATENT EXAMINER